EVALUATION KIT AVAILABLE

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MAX14850 Six-Channel Digital Isolator

General Description

The MAX14850 is a six-channel digital isolator utilizing Maxim's proprietary process technology, whose monolithic design provides a compact and low-cost transfer of digital signals between circuits with different power domains. The technology enables low power consumption and stable high-temperature performance.

The four unidirectional channels are each capable of DC to 50Mbps, with two of the four channels passing data across the isolation barrier in each direction. The two bidirectional channels are open-drain; each capable of data rates from DC to 2Mbps.

Independent 3.0V to 5.5V supplies on each side of the isolator also make it suitable for use as a level translator. The MAX14850 can be used for isolating SPI buses, I^2C buses, RS-232, RS-485/RS-422 buses, and general-purpose isolation. When used as a bus isolator, extra channels are available for power monitoring and reset signals.

The MAX14850 is available in a narrow body,16-pin SOIC (10mm x 4mm) package (for which an evaluation kit is available) and 16-pin QSOP (3.9mm x 4.94mm) package. The packages are specified over the -40°C to +125°C temperature range.

For improved performance, refer to the MAX14851. The MAX14851 has the same functionality and pin configurations, and can be used as a footprint and functional replacement for the MAX14850.

Applications

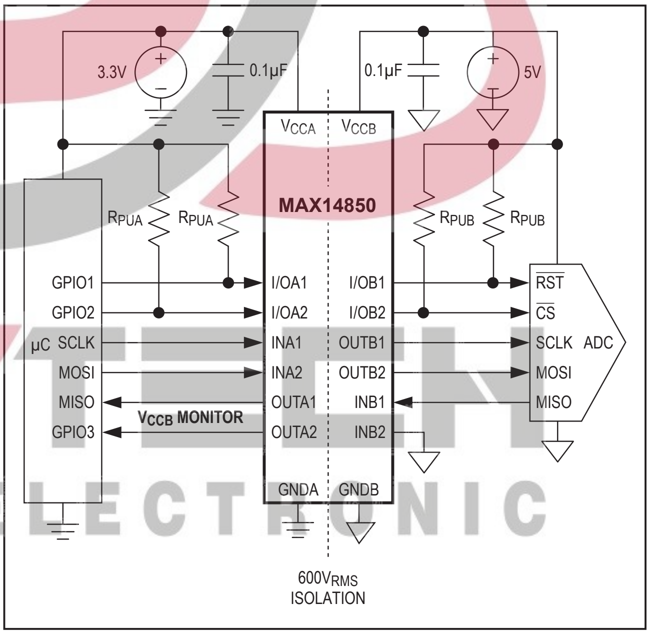
- Industrial Control Systems
- I^2C, SPI, SMBus, PMBus™ Interfaces
- Isolated RS-232, RS-485/RS-422
- Telecommunication Systems
- Battery Management
- Medical Systems

Benefits and Features

- Protection from High-Voltage Environments
  - 600V_{RMS} Isolation for 60 Seconds
  - Short-Circuit Protection on Unidirectional Outputs
  - 200V_{RMS} Working Isolation Voltage for 50 Years
- Complete Digital Isolation Solution
  - Four Unidirectional Signal Paths: 2-In/2-Out
  - Two Bidirectional Open-Drain Signal Paths
  - 50Mbps (max) Unidirectional Data Rate
  - 2Mbps (max) Bidirectional Data Rate
- Compatible with Many Interface Standards
  - I^2C
  - SPI
  - RS-232, RS-422/RS-485
  - SMBus, PMBus Interfaces

***Ordering Information* appears at end of data sheet.**

Typical Operating Circuits



PMBus is a trademark of SMIF, Inc.

Absolute Maximum Ratings

V_{CCA} to GNDA	-0.3V to +6V
V_{CCB} to GNDB	-0.3V to +6V
OUTA1, OUTA2 to GNDA	-0.3V to (V_{CCA} + 0.3V)
OUTB1, OUTB2 to GNDB	-0.3V to (V_{CCB} + 0.3V)
INA1, INA2, I/OA1, I/OA2 to GNDA	-0.3V to +6V
INB1, INB2, I/OB1, I/OB2 to GNDB	-0.3V to +6V
Short-Circuit Duration (OUTA_ to GNDA or V_{CCA}, OUTB_ to GNDB or V_{CCB})	Continuous
Continuous Current (I/OA_, I/OB_) Pin	±50mA
Continuous Power Dissipation (T_A = +70°C)	
SOIC (derate 13.3mW/°C above +70°C)	1067mW
QSOP (derate 9.6mW/°C above +70°C)	771.5mW
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 SOIC

Package Code	S16+3
Outline Number	**21-0041**
Land Pattern Number	**90-0097**
THERMAL RESISTANCE, MULTILAYER BOARD	
Junction to Ambient (θ_{JA})	75°C/W
Junction to Case (θ_{JC})	24°C/W

16 QSOP

Package Code	E16+1
Outline Number	**21-0055**
Land Pattern Number	**90-0167**
THERMAL RESISTANCE, MULTILAYER BOARD	
Junction to Ambient (θ_{JA})	103.7°C/W
Junction to Case (θ_{JC})	37°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CCA} - V_{GNDA} = 3.0V to 5.5V, V_{CCB} - V_{GNDB} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CCA} - V_{GNDA} = 3.3V, V_{CCB} - V_{GNDB} = 3.3V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNIT
DC CHARACTERISTICS								
Supply Voltage	V_{CCA}	Relative to GNDA			3.0		5.5	V
	V_{CCB}	Relative to GNDB			3.0		5.5	
Supply Current	I_{CCA}, I_{CCB}	Unidirectional inputs at DC or 2Mbps; bidirectional inputs at DC or switching at 2Mbps, no load	V_{CCA} = 5V, V_{CCB} = 5V			7.2	11	mA
			V_{CCA} = 3.3V, V_{CCB} = 3.3V			6.2	9.5	
		All inputs switching at max data rate. No load. (Note 2)	V_{CCA} = 5V, V_{CCB} = 5V	T_A = +25°C		15	22	
				T_A = +125°C		17	24	
			V_{CCA} = 3.3V, V_{CCB} = 3.3V	T_A = +25°C		10	16	
				T_A = +125°C		11	18	
Undervoltage Lockout Threshold	V_{UVLO}	V_{CCA} - V_{GNDA}, V_{CCB} - V_{GNDB} (Note 3)				2		V
Undervoltage Lockout Hysteresis	$V_{UVLOHYS}$	V_{CCA} - V_{GNDA}, V_{CCB} - V_{GNDB} (Note 3)				0.1		V
ISOLATION CHARACTERISTICS								
Isolation Voltage	V_{ISO}	t = 60s (Note 4)			600			V_{RMS}
Working Isolation Voltage	V_{IOWM}	V_{GNDB} - V_{GNDA} continuous (Note 2), 50-year life expectancy (Figure 4)					200	V_{RMS}
ESD Protection		All pins				±2.5		kV
LOGIC INPUTS AND OUTPUTS								
Input Threshold Voltage	V_{IT}	I/OA1, I/OA2, relative to GNDA			0.5		0.7	V
Input Logic-High Voltage	V_{IH}	INA1, INA2, relative to GNDA			0.7 x V_{CCA}			V
		INB1, INB2, relative to GNDB			0.7 x V_{CCB}			
		I/OA1, I/OA2, relative to GNDA			0.7			
		I/OB1, I/OB2, relative to GNDB			0.7 x V_{CCB}			
Input Logic-Low Voltage	V_{IL}	INA1, INA2, relative to GNDA					0.8	V
		INB1, INB2, relative to GNDB					0.8	
		I/OA1, I/OA2, relative to GNDA					0.5	
		I/OB1, I/OB2, relative to GNDB					0.3 x V_{CCB}	

Electrical Characteristics (continued)

(V_{CCA} - V_{GNDA} = 3.0V to 5.5V, V_{CCB} - V_{GNDB} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CCA} - V_{GNDA} = 3.3V, V_{CCB} - V_{GNDB} = 3.3V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Output Logic-High Voltage	V_{OH}	OUTA1, OUTA2, relative to GNDA, source current = 4mA		V_{CCA} - 0.4			V
		OUTB1, OUTB2, relative to GNDB, source current = 4mA		V_{CCB} - 0.4			
Output Logic-Low Voltage	V_{OL}	OUTA1, OUTA2, relative to GNDA, sink current = 4mA				0.8	V
		OUTB1, OUTB2, relative to GNDB, sink current = 4mA				0.8	
		I/OA1, I/OA2, relative to GNDA, sink current = 10mA		0.6		0.9	
		I/OA1, I/OA2, relative to GNDA, sink current = 0.5mA		0.6		0.85	
		I/OB1, I/OB2, relative to GNDB, sink current = 30mA				0.4	
Input/Output Logic-Low Threshold Difference	ΔV_{TOL}	I/OA1, I/OA2 (Note 5)		50			mV
Input Capacitance	C_{IN}	INA1, INA2, INB1, INB2, f = 1MHz			2		pF
DYNAMIC SWITCHING CHARACTERISTICS							
Common-Mode Transient Immunity	CMTI	V_{IN} = $V_{CC\_}$ or $V_{GND\_}$ (Notes 2, 6)			1.5		kV/µs
Maximum Data Rate (Note 2)	DR_{MAX}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2		50			Mbps
		I/OA1 to I/OB1, I/OA2 to I/OB2, I/OB1 to I/OA1, I/OB2 to I/OA2		2			
Minimum Pulse Width	PW_{MIN}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2 (Note 2)		20			ns
Propagation Delay (Note 2)	t_{DPLH} t_{DPHL}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2, R_L = 1MΩ, C_L = 15pF, Figure 1	V_{CCA} = V_{CCB} = 3.3V		20	30	ns
			V_{CCA} = V_{CCB} = 5V		18	26	
		I/OA1 to I/OB1, I/OA2 to I/OB2, R_1 = 1.6kΩ, R_2 = 180Ω, C_{L1} = CL2 = 15pF, Figure 2	V_{CCA} = V_{CCB} = 3.3V		30	100	
			V_{CCA} = V_{CCB} = 5V		30	100	
		I/OB1 to I/OA1, I/OB2 to I/OA2, R_1 = 1kΩ, R_2 = 120Ω, C_{L1} = C_{L2} = 15pF, Figure 2	V_{CCA} = V_{CCB} = 3.3V		60	100	
			V_{CCA} = V_{CCB} = 5V		60	100	

Electrical Characteristics (continued)

(V_{CCA} - V_{GNDA} = 3.0V to 5.5V, V_{CCB} - V_{GNDB} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CCA} - V_{GNDA} = 3.3V, V_{CCB} - V_{GNDB} = 3.3V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Pulse-Width Distortion $\lvert t_{DPLH} - t_{DPHL} \rvert$ (Notes 2, 7)	PWD	INA1 TO OUTB1, INA2 TO OUTB2, INB1 TO OUTA1, INB2 TO OUTA2, R_L = 1MΩ, C_L = 15pF, Figure 1	V_{CCA} = V_{CCB} = 3.3V			7	ns
			V_{CCA} = V_{CCB} = 5V			7	
		I/OA1 to I/OB1, I/OA2 to I/OB2, R_1 = 1.6kΩ, R_2 = 180Ω, C_{L1} = C_{L2} = 15pF, Figure 2	V_{CCA} = V_{CCB} = 3.3V			12	
			V_{CCA} = V_{CCB} = 5V			12	
		I/OB1 to I/OA1, I/OB2 to I/OA2, R_1 = 1kΩ, R_2 = 120Ω, C_{L1} = C_{L2} = 15pF, Figure 2	V_{CCA} = V_{CCB} = 3.3V			60	
			V_{CCA} = V_{CCB} = 5V			50	
Channel-to-Channel Skew (Notes 2, 7)	$t_{DSKEWCC}$	OUTB1 to OUTB2 output skew, Figure 1	V_{CCA} = V_{CCB} = 3.3V			3	ns
			V_{CCA} = V_{CCB} = 5V			3	
		OUTA1 to OUTA2 output skew, Figure 1	V_{CCA} = V_{CCB} = 3.3V			3	
			V_{CCA} = V_{CCB} = 5V			3	
		I/OB1 to I/OB2 output skew, Figure 2	V_{CCA} = V_{CCB} = 3.3V			6	
			V_{CCA} = V_{CCB} = 5V			5	
		I/OA1 to I/OA2 output skew, Figure 2	V_{CCA} = V_{CCB} = 3.3V			20	
			V_{CCA} = V_{CCB} = 5V			20	
Part-to-Part Skew (Notes 2, 7)	$t_{DSKEWPP}$	Δt_{DPLH}, Δt_{DPHL}				8	ns
Rise Time (Note 2)	t_R	OUTA1, OUTA2, OUTB1, OUTB2, 10% to 90%, Figure 1				5	ns
Fall Time (Note 2)	t_F	OUTA1, OUTA2, OUTB1, OUTB2, 90% to 10%, Figure 1				5	ns
		I/OA1, I/OA2, 90% to 10%, R_1 = 1.6kΩ, R_2 = 180Ω, C_{L1} = C_{L2} = 15pF, Figure 2	V_{CCA} = V_{CCB} = 3.3V		30	60	
			V_{CCA} = V_{CCB} = 5V		40	80	
		I/OB1, I/OB2, 90% to 10%, R_1 = 1kΩ, R_2 = 120Ω, C_{L1} = C_{L2} = 15pF, Figure 2	V_{CCA} = V_{CCB} = 3.3V		3	6	
			V_{CCA} = V_{CCB} = 5V		3	5	

Insulation and Safety Characteristics

PARAMETER	SYMBOL	CONDITIONS		VALUE	UNIT
IEC INSULATION AND SAFETY RELATED FOR SPECIFICATIONS FOR SOIC-16					
External Tracking (Creepage)	CPG	IEC 60664-1	SOIC-16	4.2	mm
			QSOP-16	3.81	mm
External Air Gap (Clearance)	CLR	IEC 60664-1	SOIC-16	4.2	mm
			QSOP-16	3.81	mm
Minimum Internal Gap		Insulation Thickness		0.0026	mm
Tracking Resistance (Comparative Tracking Index)	CTI	IEC 112 / VDE 030 Part 1		175	V
Insulation Resistance Across Barrier	R_{ISO}			1	GΩ
Capacitance Across Isolation Barrier	C_{IO}	f = 1MHz		12	pF
VDE IEC INSULATION CHARACTERISTICS					
Surge Isolation Voltage	V_{IOSM}	IEC 60747-17, section 5.3.1.6 and 5.4.6 for basic insulation		1	kVpeak
Repetitive Peak Isolation Voltage	V_{IORM}	IEC 60747-17, section 5.3.1.3		282	Vpeak
Rated Transient Isolation Voltage	V_{IOTM}	IEC 60747-17, section 5.3.1.4		850	Vpeak
Safety Limiting Temperature	T_S	IEC 60747-17, section 7.2.1		150	°C
Safety Limiting Side A Power Dissipation	P_{SA}	IEC 60747-17, section 7.2.1		0.75	W
Safety Limiting Side B Power Dissipation	P_{SB}	IEC 60747-17, section 7.2.1		0.75	W
Apparent Charge Method	q_{pd}	IEC 60747-17, section 7.4, method a & b		5	pC
Overvoltage Category		IEC 60664-1, single or three phase 50V DC or AC		I,II	—
Overvoltage Category		IEC 60664-1, single or three phase 100V DC or AC		I	—
Climatic Category				40/125/21	—
Pollution Degree		DIN VDE 0110, Table 1		2	—

Note 1: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design. All voltages of side A are referenced to GNDA. All voltages of side B are referenced to GNDB, unless otherwise noted.

Note 2: Guaranteed by design. Not production tested.

Note 3: The undervoltage lockout threshold and hysteresis guarantee that the outputs are in a known state during a slump in the supplies. See the *Detailed Description* section for more information.

Note 4: The isolation is guaranteed for t = 60s, and tested at 120% of the guaranteed value for 1s.

Note 5: $\Delta V_{TOL} = V_{OL} - V_{IL}$. This is the minimum difference between the output logic-low voltage and the input logic threshold for the same I/O pin. This ensures that the I/O channels are not latched low when any of the I/O inputs are driven low (see the *Bidirectional Channels* section).

Note 6: The common-mode transient immunity guarantees that the device will hold its outputs stable when the isolation voltage changes at the specified rate.

Note 7: Pulse-width distortion is defined as the difference in propagation delay between low-to-high and high-to-low transitions on the same channel. Channel-to-channel skew is defined as the difference in propagation delay between different channels on the same device. Part-to-part skew is defined as the difference in propagation delays (for unidirectional channels) between different devices, when both devices operate with the same supply voltage, at the same temperature and have identical package and test circuits.

Test Circuits/Timing Diagrams

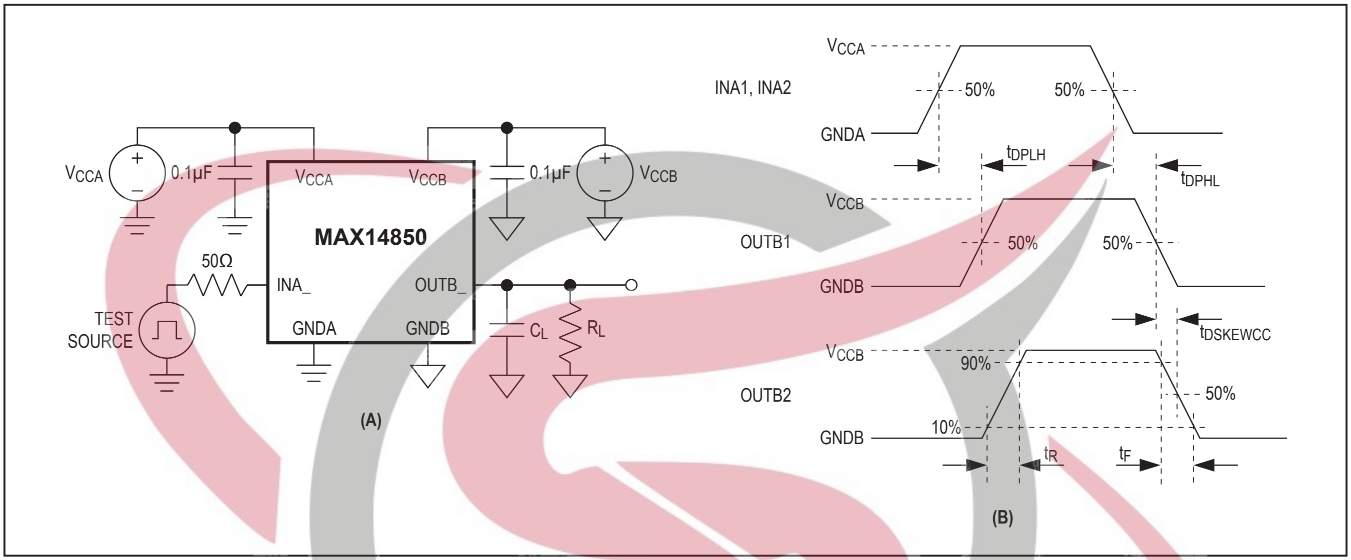


Figure 1. Test Circuit (A) and Timing Diagram (B) for Unidirectional Channels

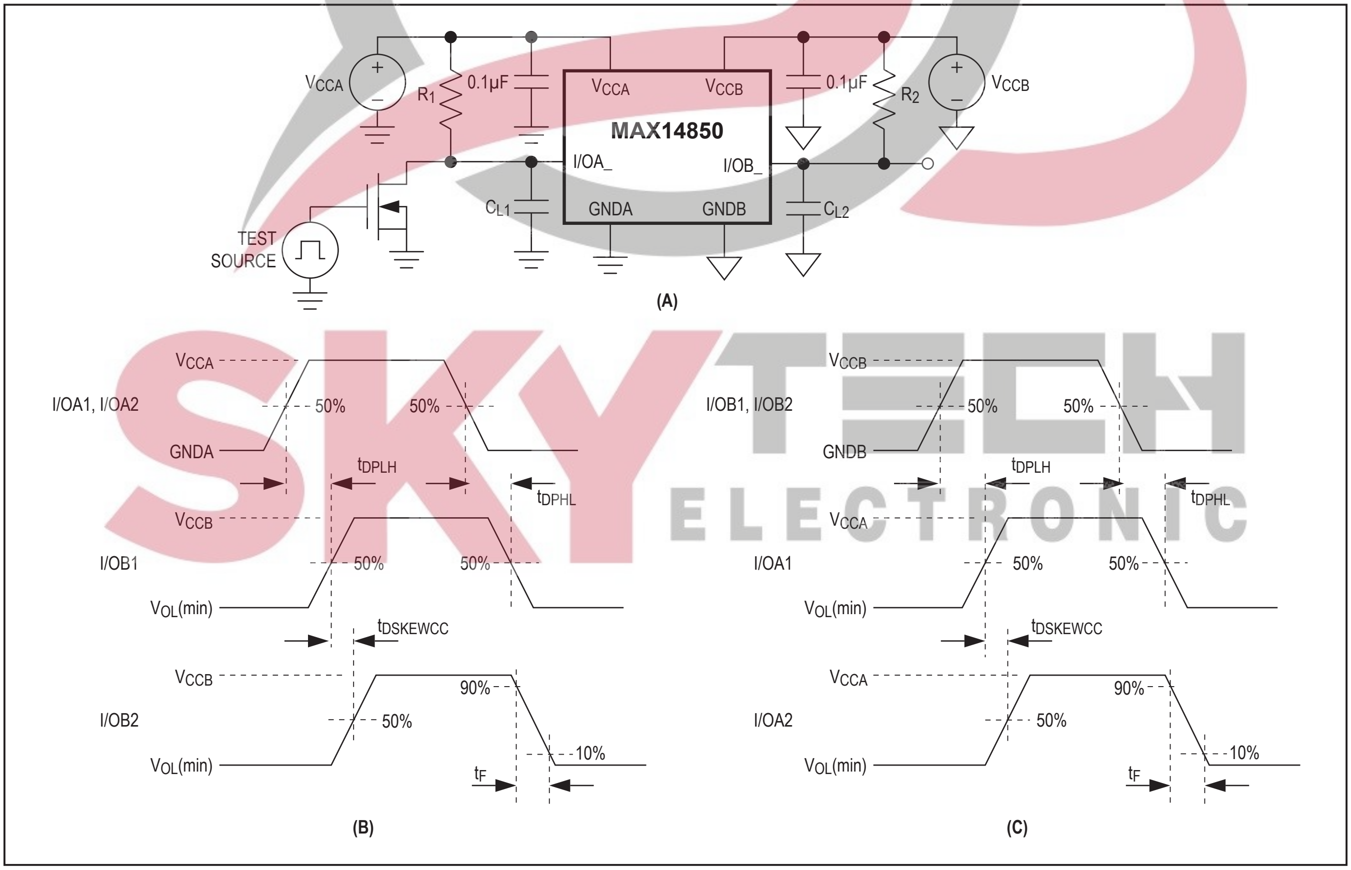
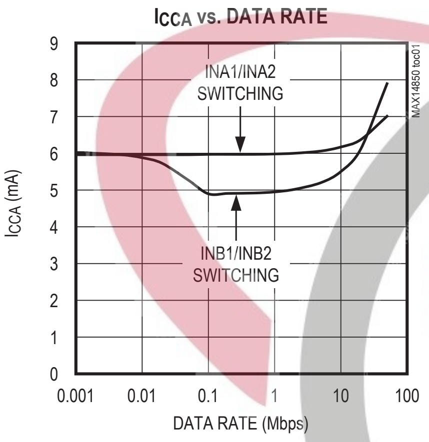
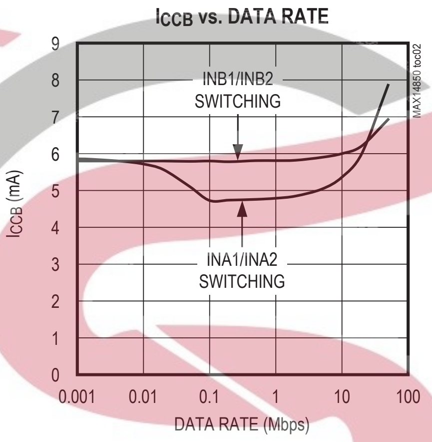


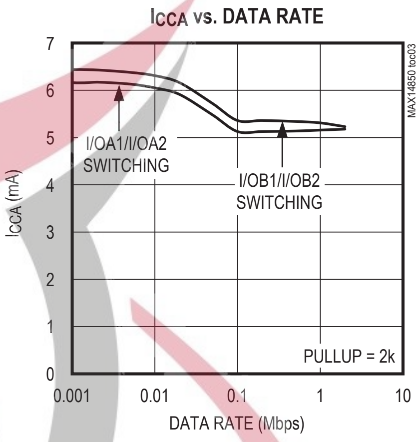
Figure 2. Test Circuit (A) and Timing Diagrams (B) and (C) for Bidirectional Channels

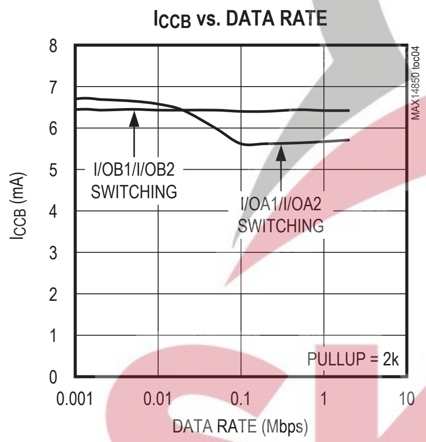
Typical Operating Characteristics

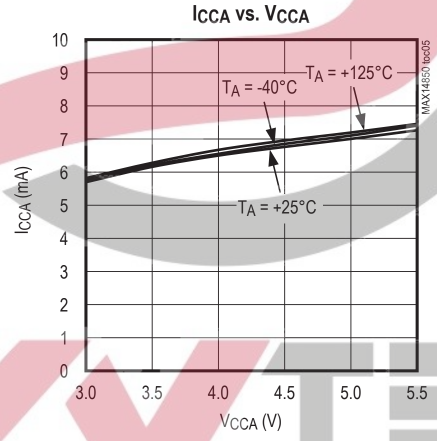
($V_{CCA} – V_{GNDA}$ = 3.3V, $V_{CCB} – V_{GNDB}$ = 3.3V, all inputs idle, T_A = +25°C, unless otherwise noted.)

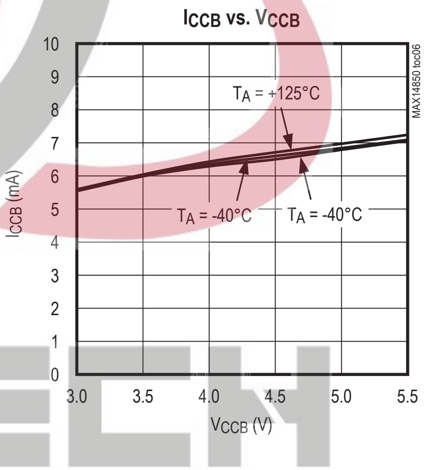

I_{CCA} vs. DATA RATE

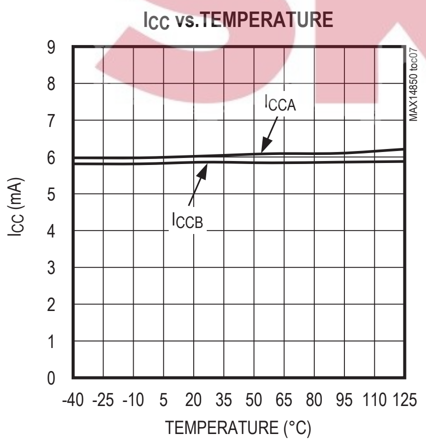

I_{CCB} vs. DATA RATE

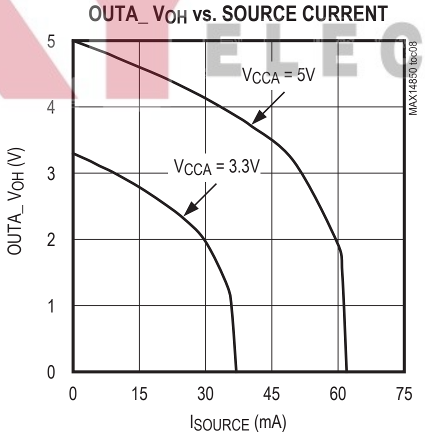

I_{CCA} vs. DATA RATE

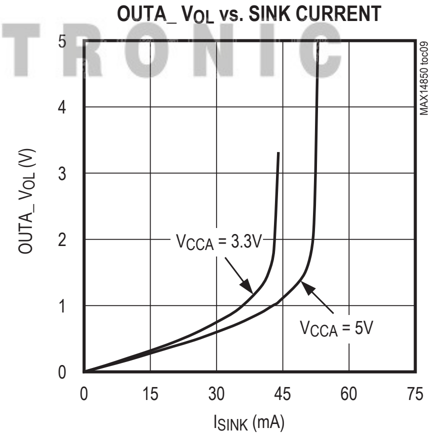

I_{CCB} vs. DATA RATE


I_{CCA} vs. V_{CCA}


I_{CCB} vs. V_{CCB}


I_{CC} vs.TEMPERATURE

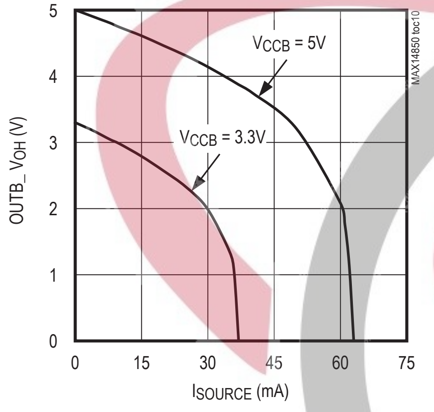

OUTA_ V_{OH} vs. SOURCE CURRENT


OUTA_ V_{OL} vs. SINK CURRENT

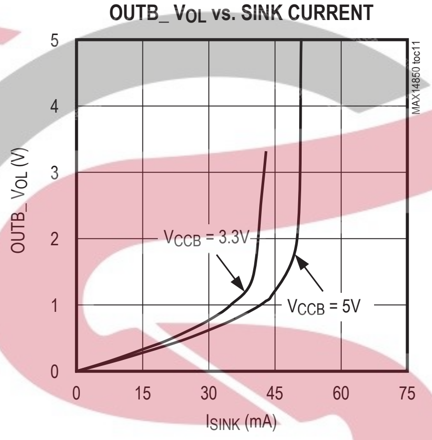
Typical Operating Characteristics (continued)

($V_{CCA} – V_{GNDA}$ = 3.3V, $V_{CCB} – V_{GNDB}$ = 3.3V, all inputs idle, T_A = +25°C, unless otherwise noted.)

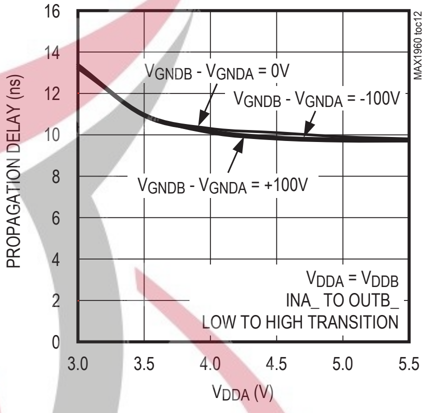
OUTB_ V_{OH} vs. SOURCE CURRENT



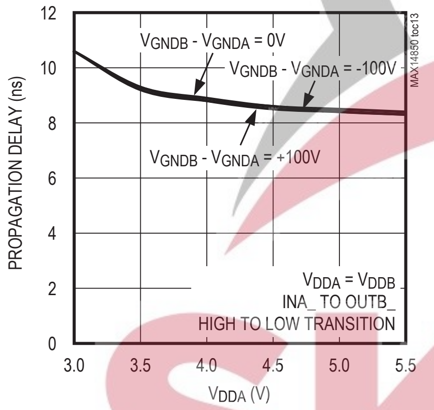
OUTB_ V_{OL} vs. SINK CURRENT



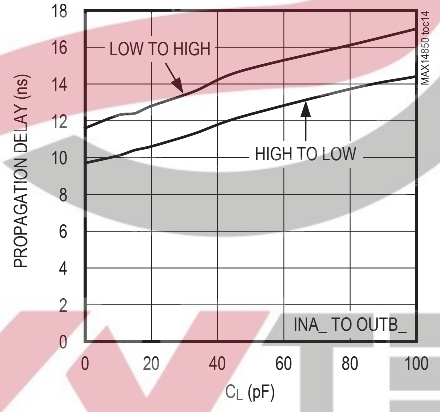
PROPAGATION DELAY vs. SUPPLY VOLTAGE



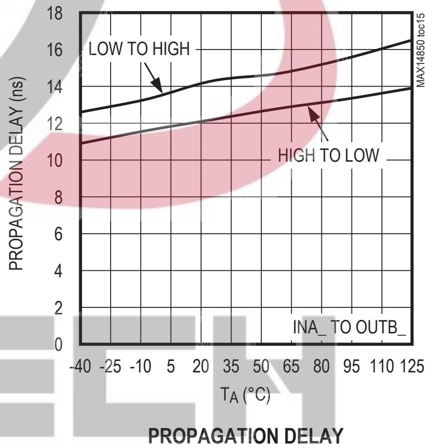
PROPAGATION DELAY vs. SUPPLY VOLTAGE



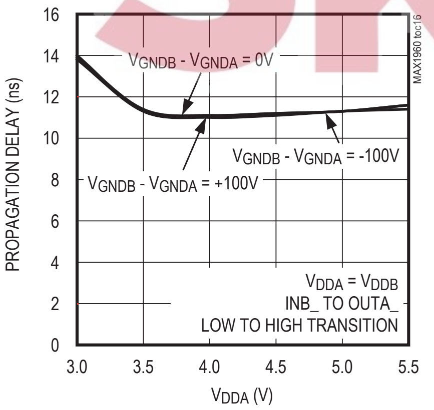
PROPAGATION DELAY vs.CAPACITIVE LOAD



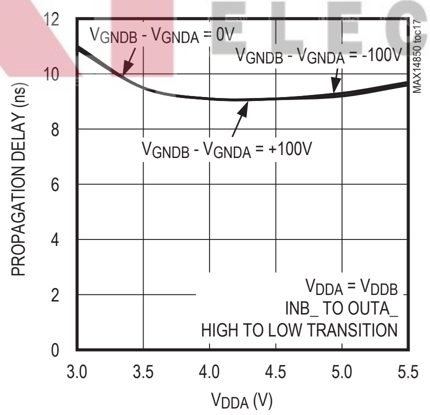
PROPAGATION DELAY vs. TEMPERATURE



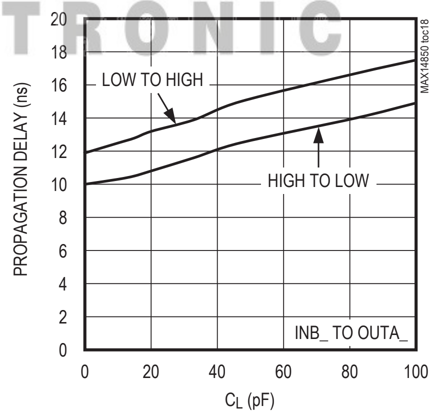
PROPAGATION DELAY vs. SUPPLY VOLTAGE



PROPAGATION DELAY vs. SUPPLY VOLTAGE



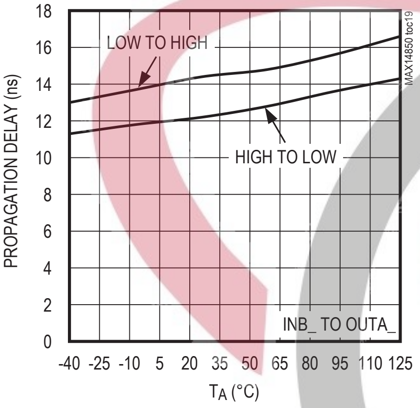
PROPAGATION DELAY vs. CAPACITIVE LOAD



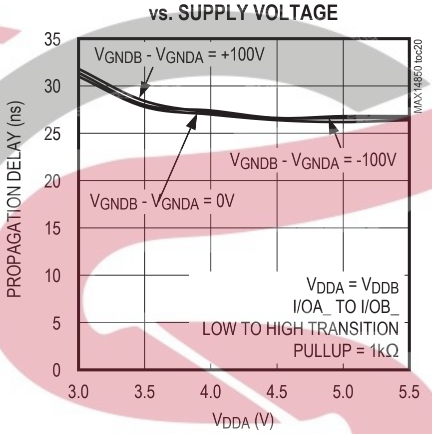
Typical Operating Characteristics (continued)

($V_{CCA} - V_{GNDA}$ = 3.3V, $V_{CCB} - V_{GNDB}$ = 3.3V, all inputs idle, T_A = +25°C, unless otherwise noted.)

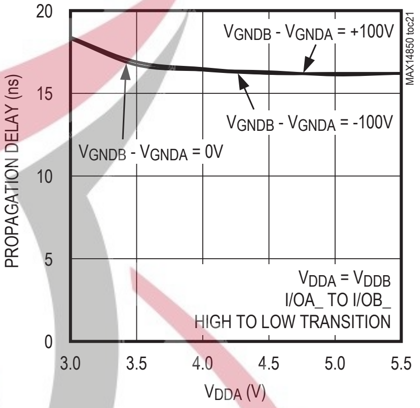
PROPAGATION DELAY
vs. TEMPERATURE



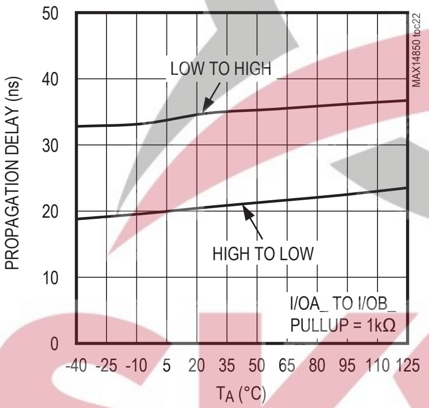
PROPAGATION DELAY
vs. SUPPLY VOLTAGE



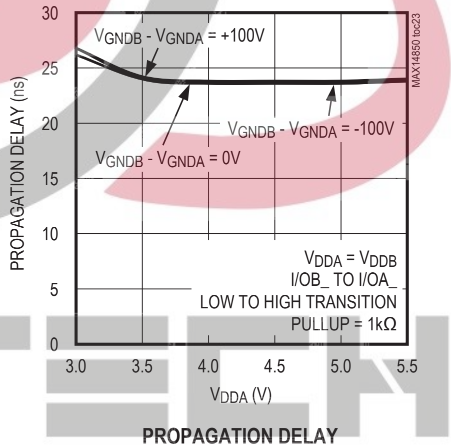
PROPAGATION DELAY
vs. SUPPLY VOLTAGE



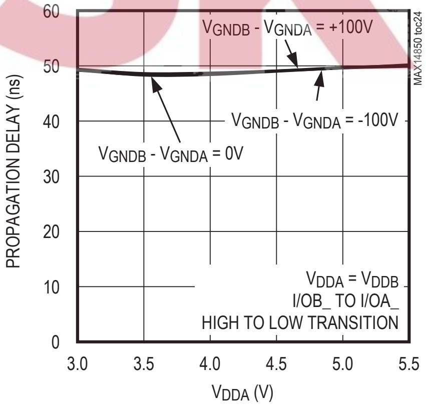
PROPAGATION DELAY
vs.TEMPERATURE



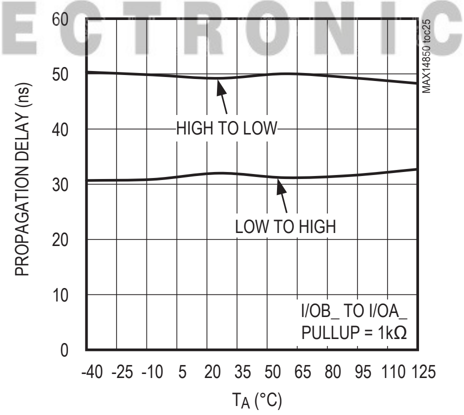
PROPAGATION DELAY
vs. SUPPLY VOLTAGE



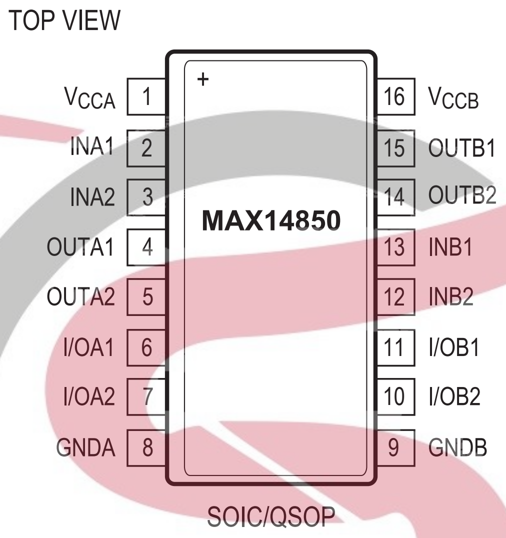
PROPAGATION DELAY
vs. SUPPLY VOLTAGE



PROPAGATION DELAY
vs. TEMPERATURE



Pin Configuration



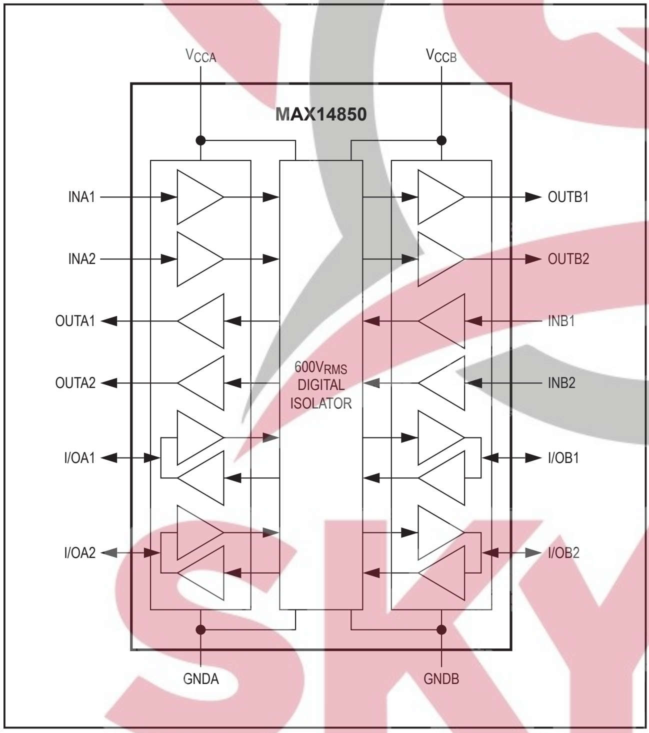
Pin Description

PIN	NAME	FUNCTION	REFERENCE
1	V_{CCA}	Supply Voltage of Logic Side A. Bypass V_{CCA} with a 0.1µF ceramic capacitor to GNDA.	GNDA
2	INA1	Logic Input 1 on Side A. INA1 is translated to OUTB1.	GNDA
3	INA2	Logic Input 2 on Side A. INA2 is translated to OUTB2.	GNDA
4	OUTA1	Logic Output 1 on Side A. OUTA1 is a push-pull output.	GNDA
5	OUTA2	Logic Output 2 on Side A. OUTA2 is a push-pull output.	GNDA
6	I/OA1	Bidirectional Input/Output 1 on Side A. I/OA1 is translated to/from I/OB1 and is a open-drain output.	GNDA
7	I/OA2	Bidirectional Input/Output 2 on Side A. I/OA2 is translated to/from I/OB2 and is a open-drain output.	GNDA
8	GNDA	Ground Reference for Side A	—
9	GNDB	Ground Reference for Side B	—
10	I/OB2	Bidirectional Input/Output 2 on Side B. I/OB2 is translated to/from I/OA2 and is a open-drain output.	GNDB

Pin Description (continued)

PIN	NAME	FUNCTION	REFERENCE
11	I/OB1	Bidirectional Input/Output 1 on Side B. I/OB1 is translated to/from I/OA1 and is a open-drain output.	GNDB
12	INB2	Logic Input 2 on Side B. INB2 is translated to OUTA2.	GNDB
13	INB1	Logic Input 1 on Side B. INB1 is translated to OUTA1.	GNDB
14	OUTB2	Logic Output 2 on Side B. OUTB2 is a push-pull output.	GNDB
15	OUTB1	Logic Output 1 on Side B. OUTB1 is a push-pull output.	GNDB
16	V_{CCB}	Supply Voltage of Logic Side B. Bypass V_{CCB} with a 0.1µF ceramic capacitor to GNDB.	GNDB

Functional Diagram



Detailed Description

The MAX14850 is a six-channel digital isolator. The device is rated for 600V_{RMS} isolation voltage for 60 seconds. This digital isolator offers a low-power, low-cost, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The device uses a monolithic solution to isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. Four of the six channels are unidirectional, two in each direction. All four unidirectional channels support data rates of up to 50Mbps. The other two channels are bidirectional with data rates up to 2Mbps.

Isolation of I^2C, SPI/MICROWIRE®, and other serial busses can be achieved with the MAX14850. The device features two supply inputs, V_{CCA} and V_{CCB}, that independently set the logic levels on either side of the device. V_{CCA} and V_{CCB} are referenced to GNDA and GNDB, respectively. The MAX14850 features a refresh mode to ensure accuracy of data when the inputs are DC.

Digital Isolation

The MAX14850 provides galvanic isolation for digital signals that are transmitted between two ground domains. Up to 200V_{RMS} of continuous isolation is supported as well as transient differences of up to 850V.

MICROWIRE is a registered trademark of Texas Instruments.

Level Shifting

The MAX14850 tolerates a ground difference of $600V_{RMS}$. Therefore, V_{GNDA} can be $850V_{DC}$ higher or lower than V_{GNDB}. In addition, the device translates logic levels when (V_{CCA}–V_{GNDA}) is higher or lower voltage than (V_{CCB}–V_{GNDB}), as long as each is within the valid 3.0V to 5.5V range.

Unidirectional and Bidirectional Channels

The MAX14850 operates both as a unidirectional device and bidirectional device simultaneously. Each unidirectional channel can only be used in the direction shown in the functional diagram. The bidirectional channels function without requiring a direction control input.

Unidirectional Channels

The device features four unidirectional channels that operate independently with guaranteed data rates from DC to 50Mbps. The output driver of each unidirectional channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Bidirectional Channels

The device features two bidirectional channels that have open-drain outputs. The bidirectional channels do not require a direction control input. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the device. I/OA1 and I/OA2 outputs comprise special buffers that regulate the logic-low voltage at approximately 0.7V. The input logic-low threshold (V_{IT}) of I/OA1 and I/OA2 is at least 50mV lower than the output logic-low voltage of I/OA1 and I/OA2. This prevents an output logic-low on side A from being accepted as an input low and subsequently transmitted to side B, thus preventing a latching action. I/OB1 and I/OB2 are conventional outputs that do not regulate the logic-low output voltage.

Due to their nature, the MAX14850 A-side output buffers cannot be connected together or to a device with similar buffers or rise time accelerators. However, the MAX14850 B-side output buffers can be connected together or to any other bidirectional buffer or level translator.

The I/OA1, I/OA2, I/OB1, and I/OB2 pins have open-drain outputs, requiring pullup resistors to their respective supplies for logic-high outputs. The output low voltages are guaranteed for sink currents of up to 30mA for side B, and 10mA for side A (see the *Electrical Characteristics* table).

Startup and Undervoltage Lockout

The V_{CCA} and V_{CCB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a slump in the supplies. When an undervoltage event is detected on either of the supplies, all outputs on both sides are automatically controlled, regardless of the status of the inputs. The bidirectional outputs become high impedance and are pulled high by the external pullup resistor on the open-drain output. The unidirectional outputs are pulled high internally to the voltage of the V_{CCA} or V_{CCB} supply during undervoltage conditions.

When an undervoltage condition is detected on either supply, all unidirectional outputs are pulled to the supplies (Table 1). The bidirectional outputs are high impedance and pulled to the supplies by the external pullup resistors. Figure 3 shows the behavior of the outputs during power-up and power-down.

Safety Regulatory Approvals

The MAX14850 is safety certified by UL, CSA, and IEC 60747-5-2. Per UL1577, the MAX14850 is 100% tested at an equivalent V_{ISO} of $720V_{RMS}$ for one second (see Table 2).

Table 1. Output Behavior During Undervoltage Conditions

V_{IN}	V_{CCA}	V_{CCB}	$V_{OUTA\_}$	$V_{OUTB\_}$
1	Powered	Powered	1	1
0	Powered	Powered	0	0
X	Undervoltage	Powered	Follows V_{CCA}	1
X	Powered	Undervoltage	1	Follows V_{CCB}

Table 2. Safety Regulatory Approvals

SAFETY AGENCY	STANDARD	ISOLATION NUMBER	FILE NUMBER
UL	UL1577 Recognized	$600V_{RMS}$ isolation voltage for 60 seconds	E351759

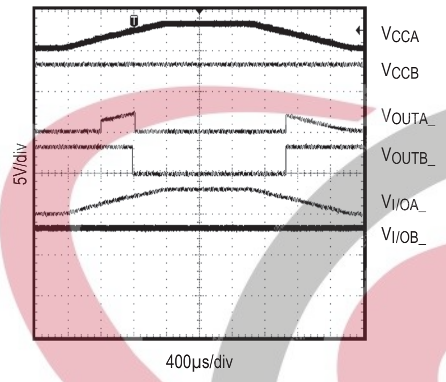


Figure 3. Undervoltage Lockout Behavior

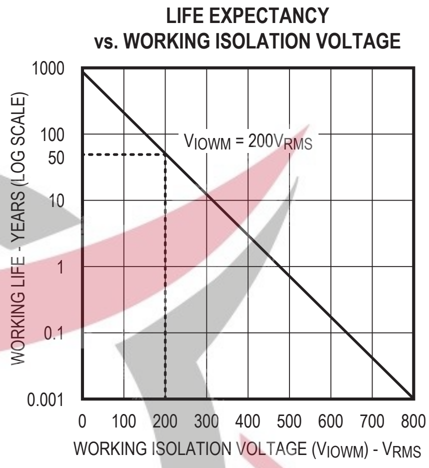


Figure 4. Life Expectancy vs. Working Isolation Voltage

Applications Information

Affect of Continuous Isolation on Lifetime

High-voltage conditions cause insulation to degrade over time. Higher voltages result in faster degradation. Even the high-quality insulating material used in the MAX14850 can degrade over long periods of time with a constant high-voltage across the isolation barrier. Figure 4 shows the life expectancy of the MAX14850 vs. working isolation voltage.

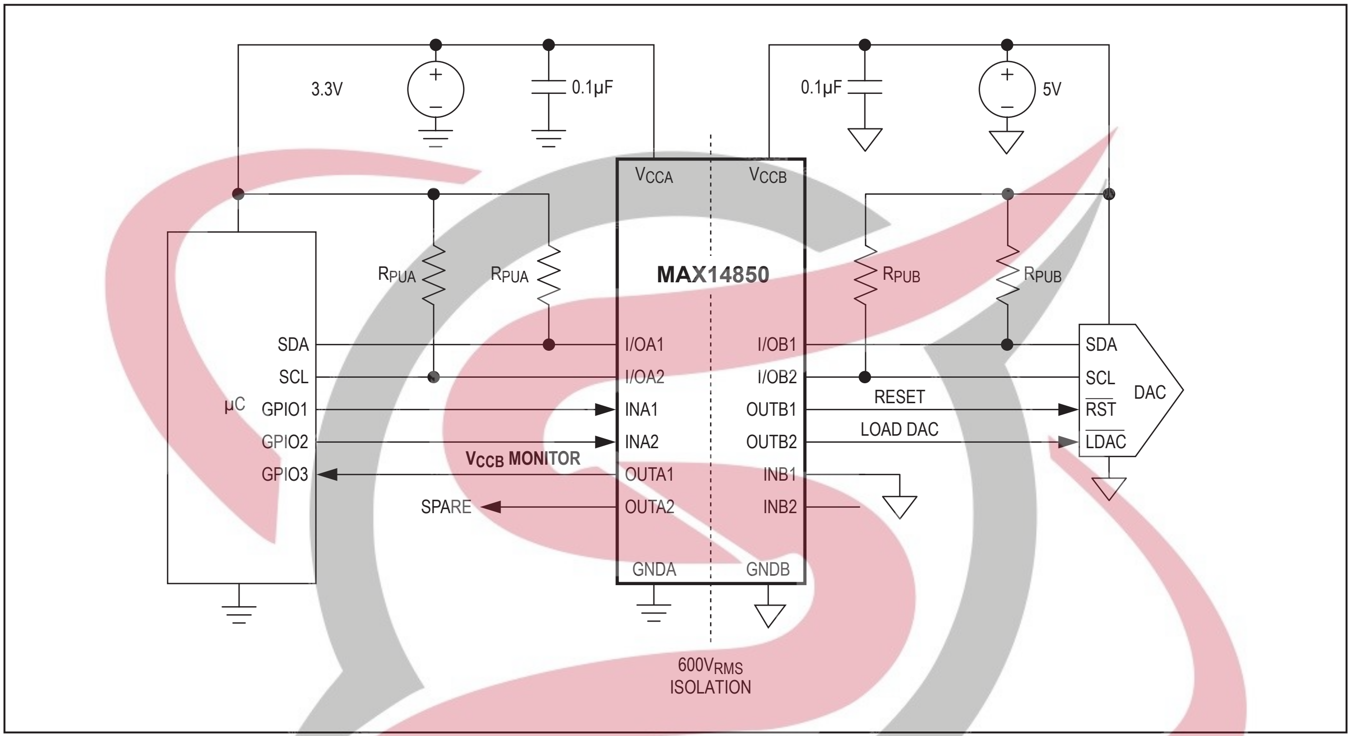
Power Supply Sequencing

The MAX14850 does not require special power-supply sequencing. The logic levels are set independently on either side by V_{CCA} and V_{CCB}. Each supply can be present over the entire specified range regardless of the level or presence of the other.

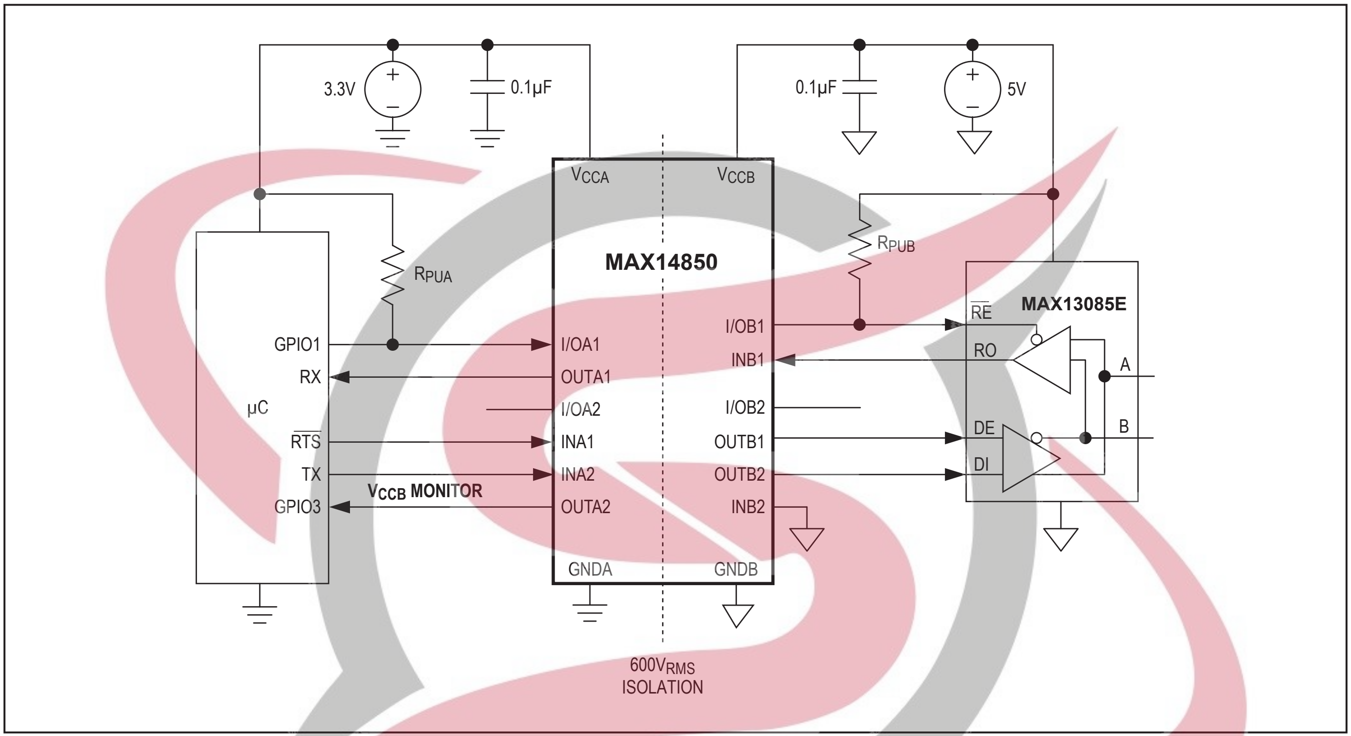
Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{CCA} and V_{CCB} with 0.1µF ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

Typical Operating Circuits (continued)



Typical Operating Circuits (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14850ASE+	-40°C to +125°C	16 SOIC
MAX14850ASE+T	-40°C to +125°C	16 SOIC
MAX14850AEE+	-40°C to +125°C	16 QSOP
MAX14850AEE+T	-40°C to +125°C	16 QSOP

+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape and Reel

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/12	Initial release	—
1	5/14	Updated *General Description*, *Benefits and Features*, *Bidirectional Channels* section, Table 2, and *Typical Operating Circuits*	1, 13, 15, 16
2	11/14	Added QSOP package and related information Additional package and ordering information for QSOP	1, 2, 6, 11, 13, 16
3	9/19	Updated *General Description*, *Absolute Maximum Ratings*, *Electrical Characteristics*, *Pin Description* table, *Level Shifting*, *Bidirectional Channels*, *Startup and Undervoltage Lockout*, *Safety Regulatory Approvals*, and Table 2.	1–3, 11–13

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.